

Programmable Phase Locked Loop Surface Mount Module

Applications	Application Notes
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- Telecommunications
- Satellite
- Telemetry

- AN-107: Manual Soldering Technique
- AN-202: Programming Z-COMM PLLs

Performance Specifications	Min	Typ	Max	Units
Frequency	163.84		163.84	MHz
Phase Noise @ 10 kHz offset (1 Hz BW)		-102		dBc/Hz
Harmonic Suppression (2nd)		-10		dBc
Spurious Suppression		-70		dBc
Power Output	-3	0	+3	dBm
Load Impedance		50		Ω
Step Size		80		kHz
Phase Detector Frequency		80		kHz
Settling Time		5		mS
Charge Pump Output Current		1250		μA
Operating Temperature Range	-40		85	°C
Package Style		CPLL		

Power Supply Requirements	Min	Typ	Max	Units
Supply Voltage 1: PLL (Vcc, nom)		3		Vdc
Supply Voltage 2: VCO (Vcc, nom)		N/A		Vdc
Supply Current 1: PLL (Icc, typ)		30		mA
Supply Current 2: VCO (Icc, typ)		N/A		mA

Reference Oscillator Signal	Min	Typ	Max	Units
Frequency		10		MHz
Phase Noise @1 kHz Offset		-145		dBc/Hz

Additional Notes

Phase Locked Loop Internal IC: Analog Devices / ADF4001

LFSuffix = RoHS Compliant. All specifications are subject to change without notice.

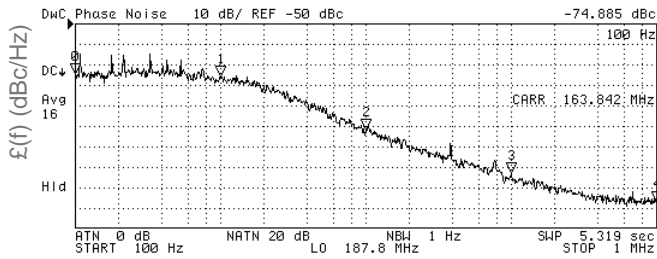
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Surface Mount Module

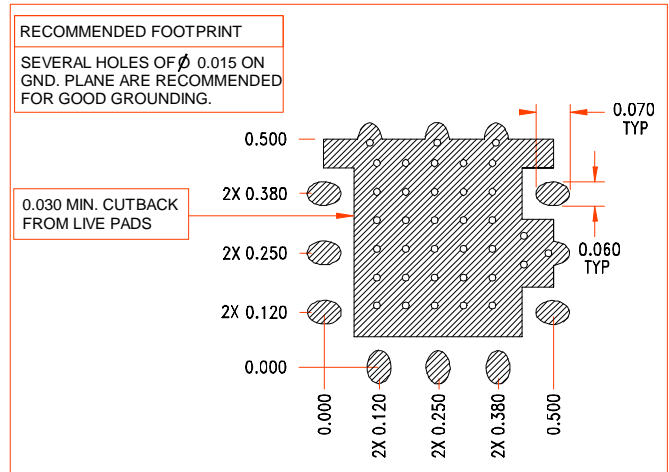
Phase Noise, typ.

PHASE NOISE (1 Hz BW, typical)

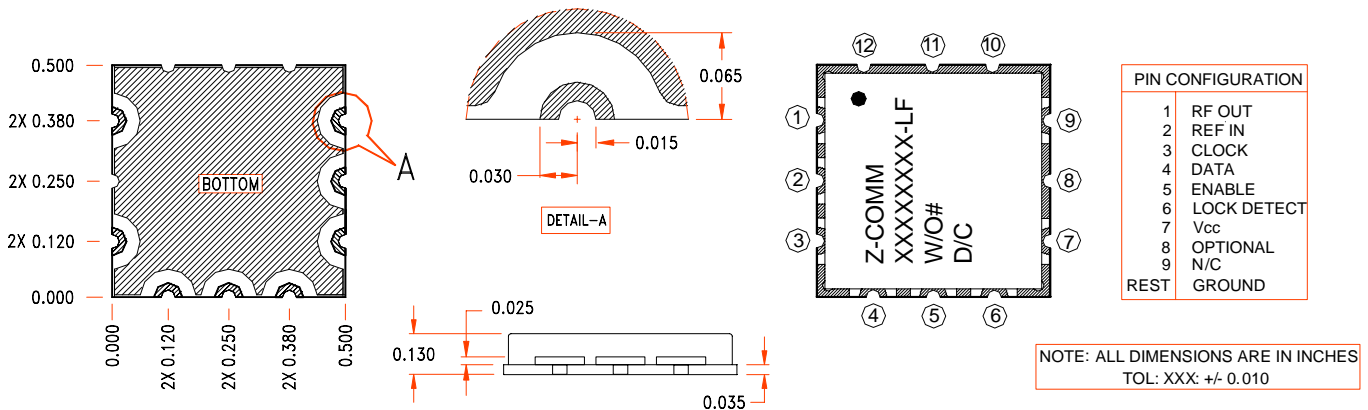
Footprint



OFFSET (Hz)



Physical Dimensions



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