

Programmable Phase Locked Loop Surface Mount Module

Applications	Application Notes
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| <ul style="list-style-type: none"> Satellite Modems Test Instrumentation | <ul style="list-style-type: none"> AN-107: Manual Soldering Technique AN-202: Programming Z-COMM PLLs |
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Performance Specifications	Min	Typ	Max	Units
Frequency	470		520	MHz
Phase Noise @ 10 kHz offset (1 Hz BW)		-97		dBc/Hz
Harmonic Suppression (2nd)		-10		dBc
Spurious Suppression		-65		dBc
Power Output	1	4	7	dBm
Load Impedance		50		Ω
Step Size		100		kHz
Phase Detector Frequency		100		kHz
Settling Time		3		mS
Charge Pump Output Current		3750		μ A
Operating Temperature Range	-40		85	$^{\circ}$ C
Package Style		CPLL		

Power Supply Requirements	Min	Typ	Max	Units
Supply Voltage 1: PLL (Vcc, nom)		3.3		Vdc
Supply Voltage 2: VCO (Vcc, nom)		N/A		Vdc
Supply Current 1: PLL (Icc, typ)		35		mA
Supply Current 2: VCO (Icc, typ)		N/A		mA

Reference Oscillator Signal	Min	Typ	Max	Units
Frequency		10		MHz
Phase Noise @1 kHz Offset		-145		dBc/Hz

Additional Notes

Phase Locked Loop Internal IC: Analog Devices / ADF4113

LFSuffix = RoHS Compliant. All specifications are subject to change without notice.

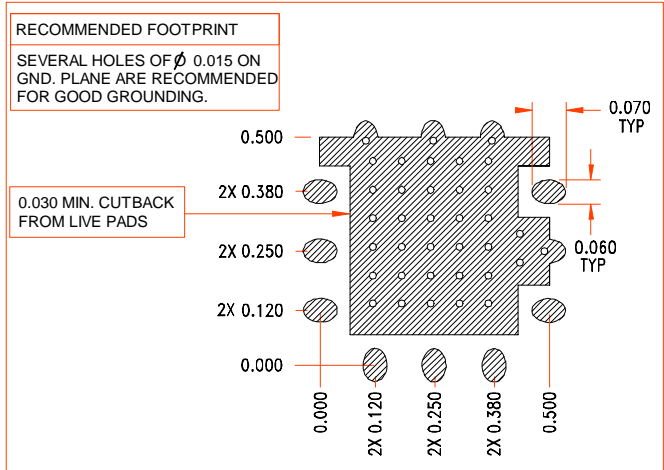
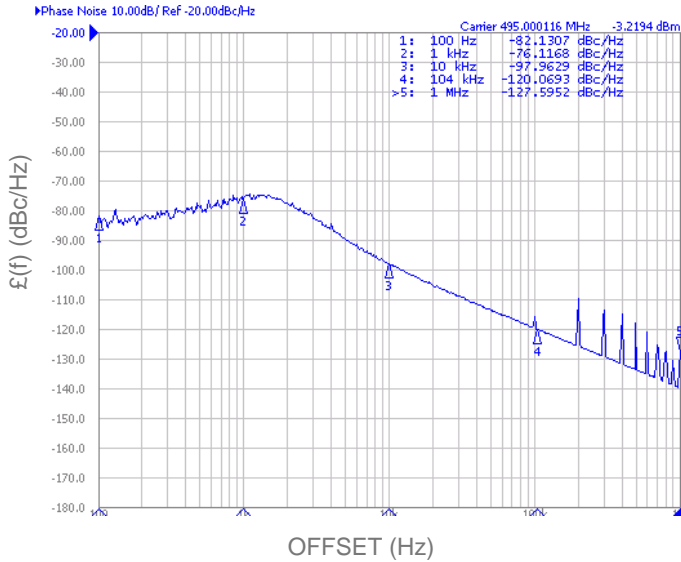
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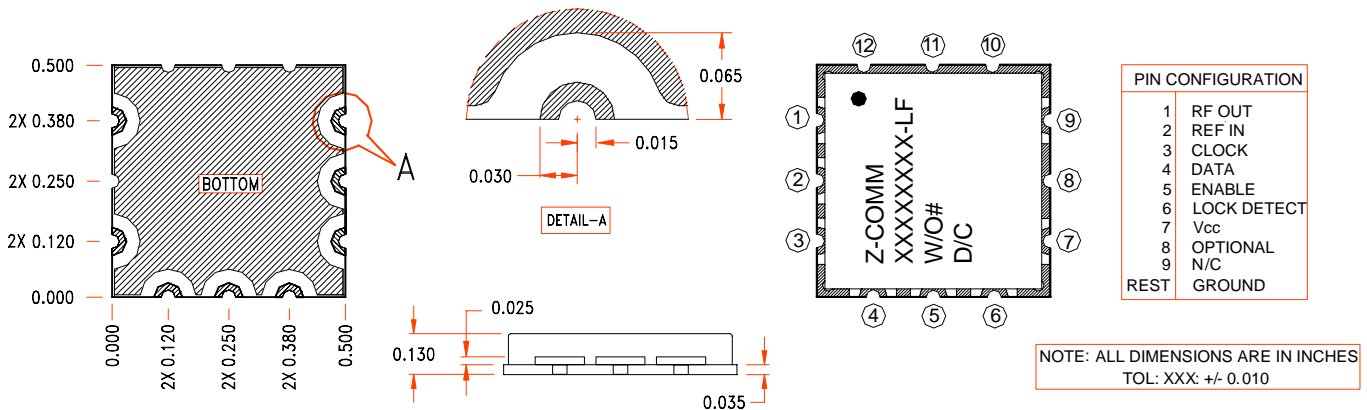
Phase Noise, typ.

Footprint

PHASE NOISE (1 Hz BW, typical)



Physical Dimensions



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