

## Programmable Phase Locked Loop Surface Mount Module

Applications	Application Notes
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|---|---|
| <ul style="list-style-type: none"> <li>Telecommunications</li> <li>Satellite Communication</li> <li></li> </ul> | <ul style="list-style-type: none"> <li>AN-107: Manual Soldering Technique</li> <li>AN-202: Programming Z-COMM PLLs</li> </ul> |
|---|---|

Performance Specifications	Min	Typ	Max	Units
Frequency	3580		3620	MHz
Phase Noise @ 10 kHz offset (1 Hz BW)		-102		dBc/Hz
Harmonic Suppression (2nd)		-15		dBc
Spurious Suppression		-70		dBc
Power Output	-3	0	3	dBm
Load Impedance		50		$\Omega$
Step Size		500		kHz
Phase Detector Frequency		500		kHz
Settling Time		1.5		mS
Charge Pump Output Current		2500		$\mu$ A
Operating Temperature Range	-40	25	85	$^{\circ}$ C
Package Style		PLL-24H		

Power Supply Requirements	Min	Typ	Max	Units
Supply Voltage 1: PLL (Vcc, nom)		5		Vdc
Supply Voltage 2: VCO (Vcc, nom)		N/A		Vdc
Supply Current 1: PLL (Icc, typ)		31		mA
Supply Current 2: VCO (Icc, typ)		N/A		mA

Reference Oscillator Signal	Min	Typ	Max	Units
Frequency		10		MHz
Phase Noise @1 kHz Offset		-145		dBc/Hz

Additional Notes
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Phase Locked Loop Internal IC: Analog Devices / ADF4106

LFSuffix = RoHS Compliant. All specifications are subject to change without notice.

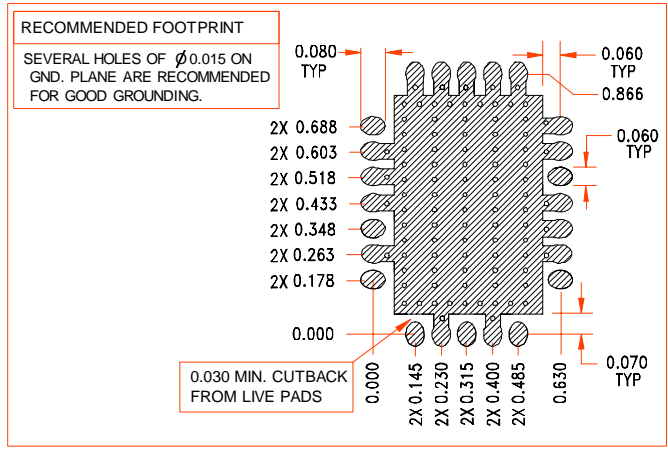
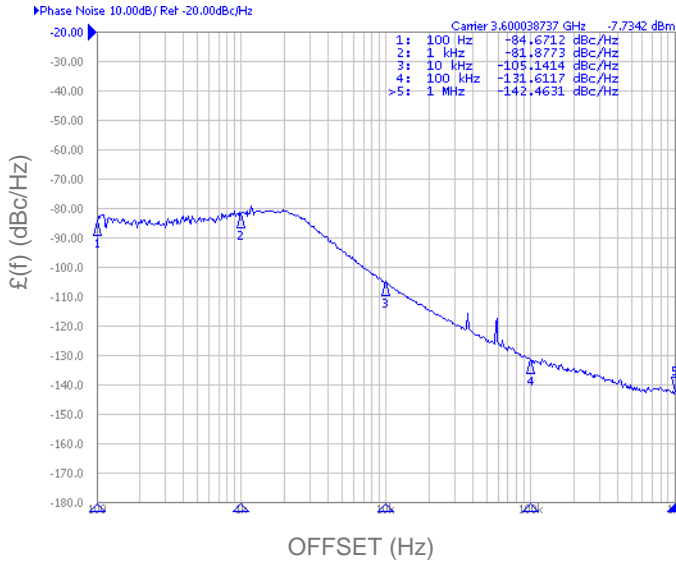
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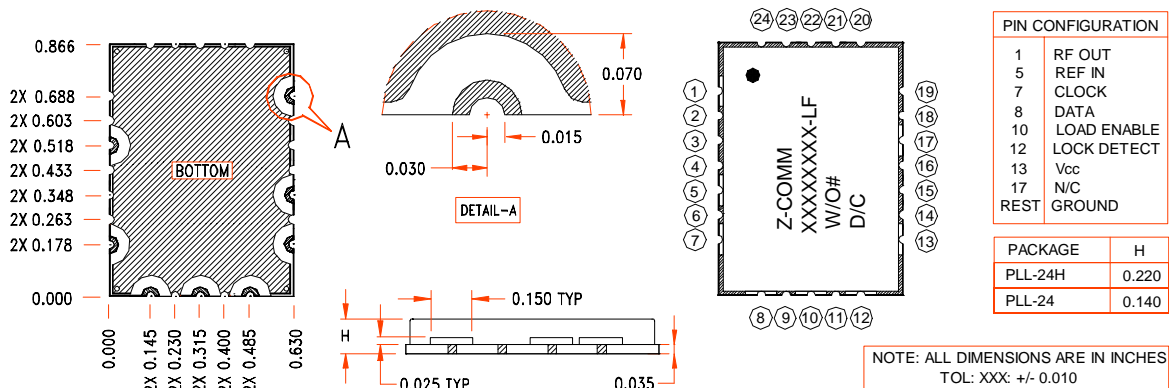
### Phase Noise, typ.

### Footprint

PHASE NOISE (1 Hz BW, typical)



### Physical Dimensions



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