Programming Z-COMM Phase Locked Loops

Nomenclature
Z-COMM has three models of Phase Locked Loops available, each using either the National Semiconductor or the Analog Devices PLL synthesizer chip.

PSNxxxxx:	Phase Locked Loop, Standard Package (0.6" x 0.9"), National Semiconductor.
PSAxxxxx:	Phase Locked Loop, Standard Package, Analog Devices.
PCAxxxxx:	Phase Locked Loop, Compact Package (0.5" x 0.5"), Analog Devices.

This application note will cover the programming techniques of each of Z-COMM's Phase Locked Loops.

Compact Package Pin Description

P1	RF Output
P2	Reference Oscillator Input
P3	Clock
P4	Data
P5	Load Enable
P6	Lock Detect
P7	Vcc
P8	No Connection
P9	No Connection
P10-12	Ground

Standard Package Pin Description

P1	*P1	RF Output
P2	P2-4	Ground
P3	P5	Reference Oscillator Input
P4	P7	Clock
P5	P8	Data
P6	P10	Load Enable
P7	P12	Lock Detect
P8	P13	Vcc
P9	P14-16	Ground
P10	P17	No Connection
P11-14	P18-24	Ground

**Pin out for PLL-24 Standard Package*

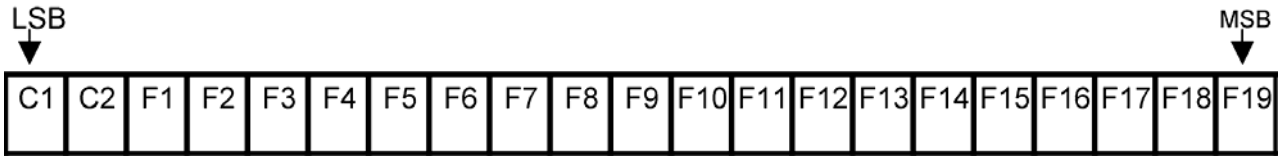
Each of the PLL synthesizers includes the reference divider (R counter), phase detector, charge pump, and the main divider (N counter). Z-COMM provides the completed PLL with the inclusion of the loop filter and the VCO into the PLL module. Typically the end user supplies the crystal reference.

Does your PLL have a National Semiconductor synthesizer chip?

Z-COMM uses the LMX2306, 2316, and the 2326 PLL synthesizer chips. Please refer to the data sheet for your PLL to find out which one is used.

National Semiconductor uses a 21-bit shift register to load data via a 3 wire connect. These correspond to the clock, data, and load enable pins on the PLL. See Figure 1.

Figure 1 - 21-bit shift register



The data stream is shifted into the data input on the rising edge of the clock, most significant bit first. Then the data is transferred from the shift register to one of four latches on the rising edge of load enable (LE). The first 2 bits of the register are control bits and are used to program the R counter, N counter, function latch (Fast Lock modes), or initialization. Table 1 shows the bit configuration for the 4 states.

Control		DATA Location
C1	C2	
0	0	R Counter
1	0	N Counter
0	1	Function Latch
1	1	Initialization

One now needs to determine the frequencies and mode of operation. The National PLL synthesizer provides 5 modes of operation, 4 Fast Lock modes, and a normal operation mode. All of Z-COMM PLLs with a National chip are built to run in normal mode only. Additional hardware in the PLL module is required to make use of the Fast Lock modes.

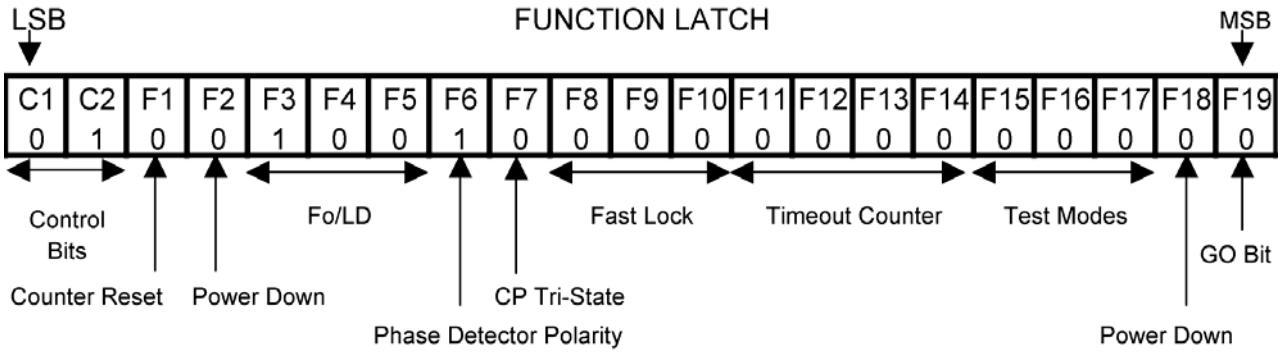
Table 1

Function Latch, R Counter, and N Counter

Function Latch:

National Semiconductor recommends, for efficient programming, that the PLL synthesizer be programmed in this specific order, function latch, R counter, and finally the N counter. Here at Z-COMM we have found this method to work very well. Figure 2, below, shows the contents of the 21-bit register Z-COMM used for the function latch.

Figure 2

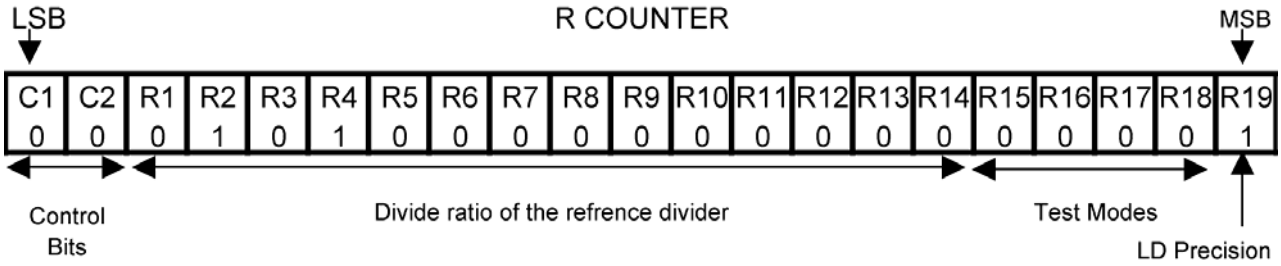


Function Description

C1, C2	Control Bits. These are configured load the function latch.
F1	Counter reset. When starting up this bit should be low to ensure that the N counter will resume counting in alignment with the R counter.
F2, F18	Power down. During normal operation these bits should be left low. For more about the synchronous and asynchronous power down modes, you can visit www.national.com.
F3-F5	Lock detect modes. Z-COMM uses the Digital Lock Detect mode (1 0 0) for testing and use with our PLL Eval Board.
F6	Phase detector polarity. A '1' signifies positive polarity. All Z-COMM PLLs require a positive phase detector polarity.
F7	Charge pump tri-state. This should be low for normal operation.
F8-17	These bits should all be set to '0' for Z-COMM PLLs. Additional hardware is required to make use of the Fast Lock modes.
F19	Go bit. This bit should be low for now. It becomes useful when programming the R and N counters, at that time this bit will be used to set the output charge pump current.

R Counter:
To load the R counter simply determine the binary equivalent of your reference divider ratio and then program the appropriate bits. Figure 3, shows the contents of the 21-bit register to properly load in a divide ratio of 10 and Lock Detect precision of 5 consecutive reference cycles.

Figure 3



The reference divider ratio is defined as:

$$R = \frac{\text{Ref. Oscillator Freq}}{\text{Compare Freq, (Step Size)}}$$

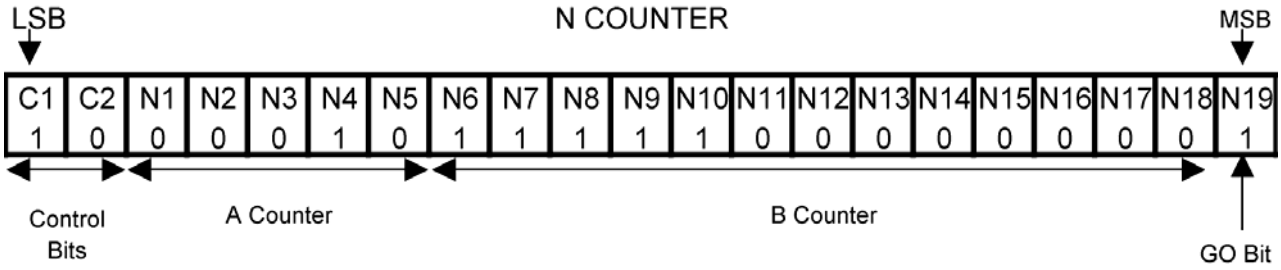
For example: $\frac{\text{10MHZ Reference}}{\text{1000KHz Step size}} = 10$ **(this value must be an integer)**

Function Description

C1, C2	Control Bits. These are configured load the R counter.
R1-14	Divide ratio of the reference divider. This ratio must be: 3 ≤ R ≤ 16383.
R15-18	Test modes. These bits should be zero for normal operation.
R19	Lock Detect Precision. When this bit is a '1' 5 consecutive reference cycles, instead of 3, will be used.

N Counter:
The N counter consists of 2 sub-counters, a 5-bit swallow counter, called the A counter, and a 13-bit B counter. This section will show how to calculate the A and B counters, and set the charge pump current. Figure 4 shows the contents of the 21-bit register to properly load in the A and the B counter for N = 1000 and charge pump current of 1mA.

Figure 4



The main divider ratio, N is defined as:

$$N = \frac{\text{Output Freq of the VCO}}{\text{Compare Freq, (Step Size)}}$$

For example: $\frac{\text{1000MHz RF output}}{\text{1000KHz Step size}} = 1000$ **(this value must be an integer)**

National Semiconductor defines N, A, and B in the following way:
N = P * B + A; where P is the value of the prescaler. Note: For Z-COMM PLLs employing the LMX2306 chip use "8" for the prescaler, for the LMX2316 and the LMX2326 use "32" for the prescaler.
B = div(N / P); where div(x) is defined as the integer portion.
A = N – (B * P)

Continuing our example:
B = div(1000 / 32) = div(31.25) = 31 = 0000000011111
A = 1000 – (31 * 32) = 8 = 01000

Function Description

C1, C2	Control Bits. These are configured load the N counter.
N1-N5	A Counter. N1 is the LSB and N5 is the MSB. **0 ≤ A ≤ 31** for the LMX2316/26, **0 ≤ A ≤ 7** for the LMX2306, and **A ≤ B** for all chips.
N6- N18	B counter. N6 is the LSB and N18 is the MSB. **3 ≤ B ≤ 8191**.
N19	GO Bit. This sets the charge pump output current. "1" high 1mA, "0" low 250µA. Please see the data sheet for your PLL to find the charge pump current setting.

A Note about Timing
The National chip has a minimum clock pulse width high and low of 50 ns, 20 MHz. This is the rate at which data is clocked into the 21-bit shift register. When the load enable bit goes high the data is latched in.

Does your PLL have an Analog Devices synthesizer chip?
As previously mentioned Z-COMM PLL products utilize Analog Devices frequency synthesizer chips. PSA and PCA part numbers denote the PLL products employing the Analog Devices chips. Please refer to the data sheet to find which chip is used.

Analog Devices uses a 24-bit shift register to load data via a 3-wire connect. These correspond to the clock, data, and load enable pins on the PLL. The data stream is shifted into the DATA input on the rising edge of the clock, most significant bit first. Then the data is transferred from the shift register to one of four latches on the rising edge of load enable (LE).

Device Programming after Initial Power-Up
After initially powering up the device there are three ways to program the device, the Initialization Latch Method, the CE Pin Method, and the Counter Reset Method. Z-COMM uses the Initialization Latch Method. The CE Pin Method cannot be used, as there is no external access to the CE pin on the PLL synthesizer, it is permanently tied high. The exploration of the Counter Reset Method is left to the end user.

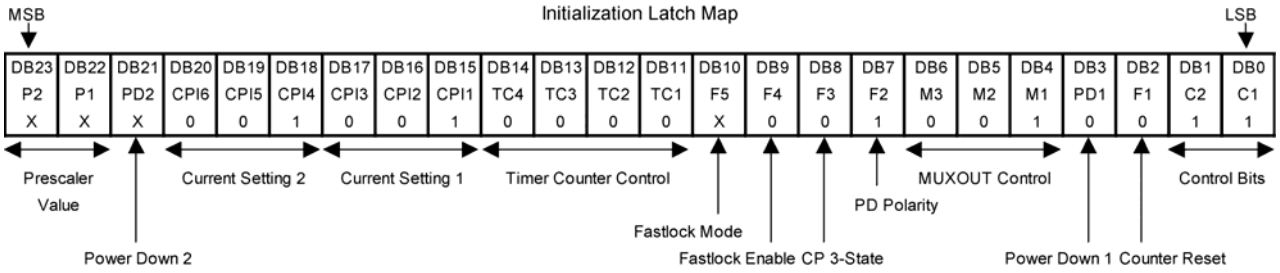
The first 2 bits of the 24-bit register are control bits and are used to program the initialization latch, R counter, N counter, and function latch. The configuration is the same as the National Semiconductor chip in table 1.

Using the Initialization Latch Method
1. Load initialization latch, '11'.
2. Load R counter, '00'.
3. Load N counter, '01'.

1. Loading the Initialization Latch

As an example Figure 5 shows the contents of the 24-bit register that Z-COMM used for the initialization latch.

Figure 5



When initializing the chip an internal pulse resets both the R, and the N counter, this will allow close phase alignment when counting resumes.

Function Description

C1, C2 — Control Bits. These must be set to "11".

F1 — Counter Reset. This bit should be low for normal operation, otherwise R and N will be held in a reset state.

PD1, PD2 — Power-Down mode. Since the CE pin is always high the following truth table will apply.

PD2	PD1	Mode
X	0	Normal operation
0	1	Asynchronous power-down
1	1	Synchronous power-down

Z-COMM employs the normal operation mode, for further assistance on the power down modes please contact Z-COMM or see Analog Devices on the web at www.analog.com.

M1-M3 — MUXOUT Control. Z-COMM uses the digital lock detect (0 0 1), other modes are available please contact Z-COMM or see Analog Devices.

F2 — Phase Detector Polarity. This bit should be high (positive) for Z-COMM PSAs and PCAs.

F3 — Charge Pump 3-State. This bit should be low for Z-COMM PSAs and PCAs.

F5-F4 — Fastlock Mode and Enable. Z-COMM does not test for any Fastlock modes and therefore these bits should be (X 0). This does not mean that the end user cannot use these modes. Please contact Z-COMM or see Analog Devices for more about the Fastlock modes.

TC4-TC1 — Timer Counter Control. When the Analog chip is in Fastlock it will remain in Fastlock until the Timer Counter Control has cycled to timeout. At that time the chip will return to a static state.

CPI6-CPI1 — Current Setting 2, and 1. Analog defines the output current in terms of an Rset resistor, 2.7K, 4.7K, and 10K-ohm. Each Z-COMM PCA and PSA uses a 4.7K-ohm resistor at the output of the charge pump. With that choice we are held to eight values of the charge pump current. Table 2 shows the bit sequences for each

setting. In figure 5 a charge pump current of 1.25 mA is selected, for example. The user will need to see the data sheet for their specific PCA or PSA to find out what the normal charge pump current settings should be. If the user had opted to use the Fastlock mode, Analog recommends that Current Setting 2 be used for the high Fastlock current and Current Setting 1 be used for the normal operating current setting. Once again, please contact Z-COMM or see Analog Devices for more about the Fastlock modes.

CPI6	CPI5	CPI4	Icp (mA) 4.7K-ohm
CPI3	CPI2	CPI1	
0	0	0	0.625
0	0	1	1.25
0	1	0	1.875
0	1	1	2.5
1	0	0	3.125
1	0	1	3.75
1	1	0	4.375
1	1	1	5

Table 2

P2, P1 Prescaler Value. For the ADF 4001 these are to be (X X), the don't care state, as the ADF 4001 does not require any prescaler value. For the ADF 411X use the following table.

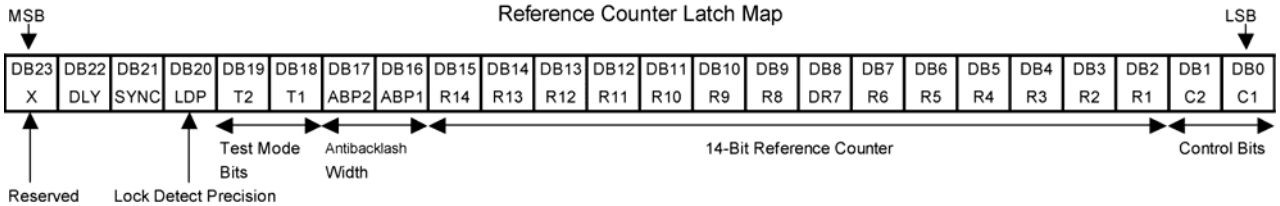
P2	P1	Prescaler Value
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 200 MHz. Thus, with an RF frequency of 2 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not.

2. Loading the R Counter

Figure 6 shows the general layout for the R counter latch map. Please note that the 14-bit reference counter and the control bits work in exactly the same way as the National Semi Conductor chip.

Figure 6



Function Description

C1, C2 Control Bits. These are configured load the R counter.

R1-14 Divide ratio of the reference divider. This ratio must be: 3 ≤ R ≤ 16383.

ABP1, 2 Antibacklash Pulse Width.

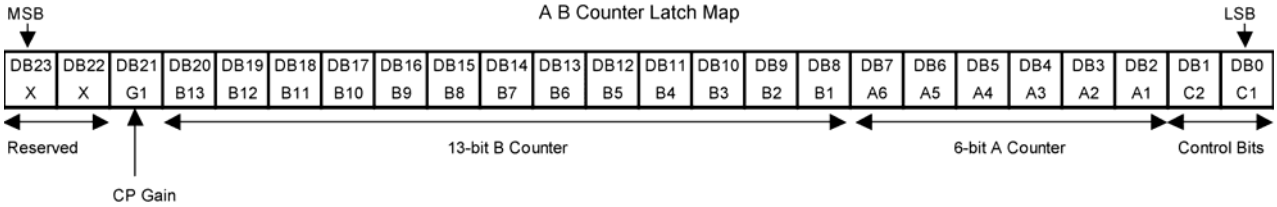
ABP2	ABP1	Pulse Width
0	0	3 ns
0	1	1.5 ns
1	0	6 ns
1	1	3 ns

T1, 2	Test modes. These bits should be zero for normal operation.
LDP	Lock Detect Precision. A low '0' three cycles occur before lock detect, high '1' 5 cycles.
SYNC	This bit should be '0' for normal operation.
DLY	This bit should be '0' for normal operation.
DB23	X = Don't care.

3. Loading the N Counter.

Figure 7 shows the general layout for the N counter latch map. Please note that the 13-bit B counter and the 6-bit A counter, swallow counter, and control bits work in the same way as the National Semi Conductor chip. Except for the A counter can have 6 bits.

Figure 7



Function Description

C1, C2	Control Bits. These are configured load the N counter.
A1-A6 A	Counter. A1 is the LSB and A6 is the MSB. 0 ≤ A ≤ 63.
B1- B13	B counter. N6 is the LSB and is the MSB. 3 ≤ B ≤ 8191. A ≤ B.
G1	Charge Pump Gain. See the following table.

F4 (F.L. ENB)	***G1***	***Operation***
0	0	CP current setting 1 is permanently used.
0	1	CP current setting 2 is permanently used.
1	0	CP current setting 1 is used.
1	1	CP current is switched to setting 2. The time spent in setting 2 is dependent on which Fastlock mode is used. Once again, please contact Z-COMM or see Analog Devices for more about the Fastlock modes.

DB22, 23	X = Don't care. The N Counter does not use these bits.

Timing the Analog Devices Chip

The Analog chip has a minimum clock pulse width high and low of 25 ns, 40 MHz. This is the rate at which data is clocked into the 24-bit shift register. When the load enable bit goes high the data is latched in.